

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization International Bureau



549291



(43) International Publication Date  
30 September 2004 (30.09.2004)

PCT

(10) International Publication Number  
WO 2004/084292 A1

(51) International Patent Classification<sup>7</sup>: H01L 21/336, 29/423, 29/786, 21/84, 27/12

(21) International Application Number:  
PCT/JP2004/003808

(22) International Filing Date: 19 March 2004 (19.03.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
2003-078002 20 March 2003 (20.03.2003) JP

(71) Applicant (for all designated States except US): MAT-SUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oaza Kadoma Kadoma-shi Osaka, 5718501 (JP).

(72) Inventors; and

(75) Inventors/Applicants (for US only): IWANAGA, Junko. TAKAGI, Takeshi. KANZAWA, Yoshihiko. SORADA, Haruyuki. SAITO, Tohru. KAWASHIMA, Takahiro.

(74) Agents: MAEDA, Hiroshi et al.; Honmachi-nakajima Bldg., 4-8, Utsubohonmachi 1-chome, Nishi-ku Osaka-shi Osaka, 5500004 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

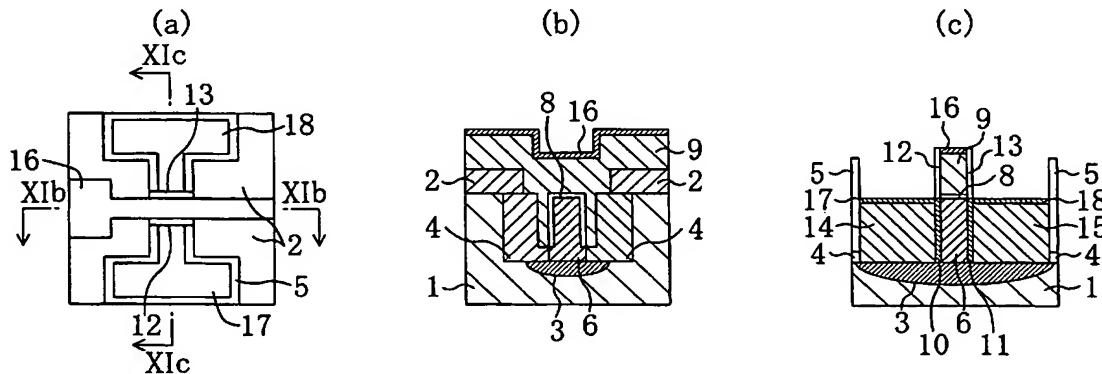
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- with amended claims

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FINFET-TYPE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME



(57) Abstract: A semiconductor device includes: a semiconductor substrate in which a trench is formed; a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type; a semiconductor FIN buried in the trench and provided between the source and drain regions; a gate insulating film provided on a side surface of the semiconductor FIN as well as the upper surface of the semiconductor FIN; and a gate electrode formed on the gate insulating film.

WO 2004/084292 A1